

Rev.	Content	Date	Name	WÜRTH Elektronik eiSos			
1.0	Original Document	01-01-2023	Nattawut				
1.1	Change to AD controller	20-04-2023	Nattawut	PoDL PD Main		Customer:	
1.2	Update Power Coupling	04-11-2023	Nattawut				
1.3	Improve for EMC ability	14-05-2024	Nattawut	Size: A3 Document Number: 00-PoDL_PD_Main.SchDoc		Modified By: Nattawut	
1.4	Add D31, Replace FB7 to R164	05-07-2024	Nattawut				
1.5	Improve for EMC ability	16-09-2024	Nattawut	Print Date : 19/09/2024		Design Date : Mon 1st Aug, 2020	Sheet: 0 of 4

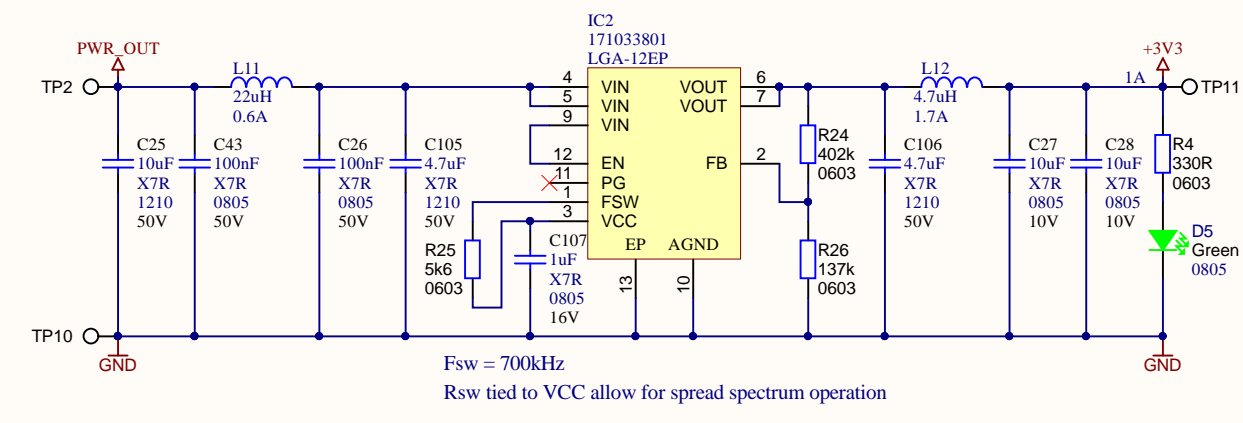
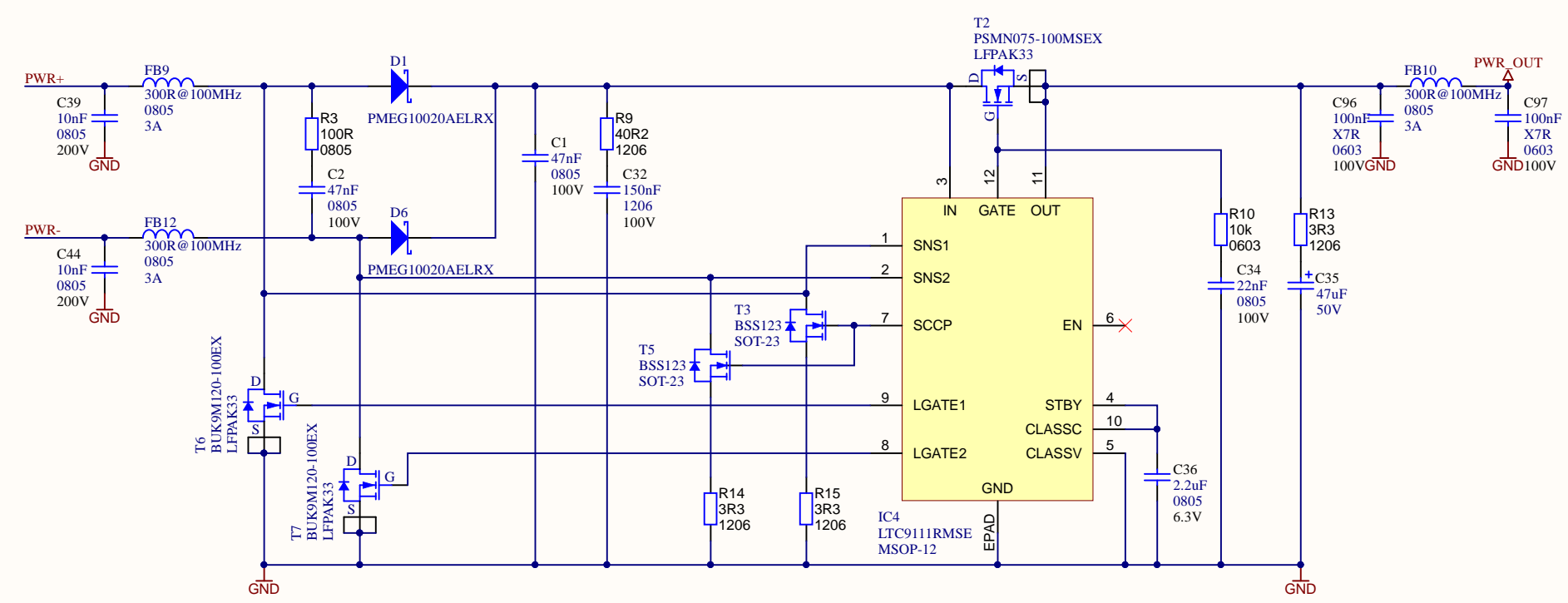
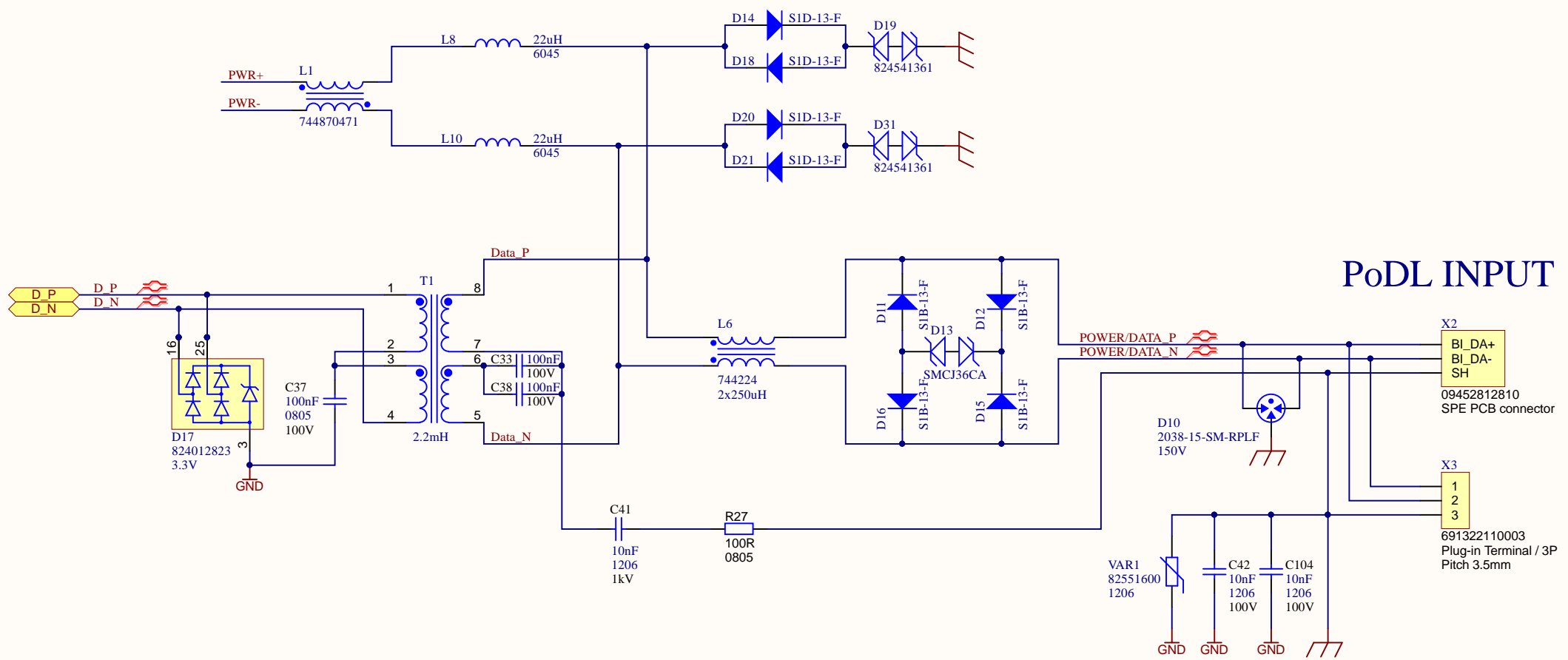
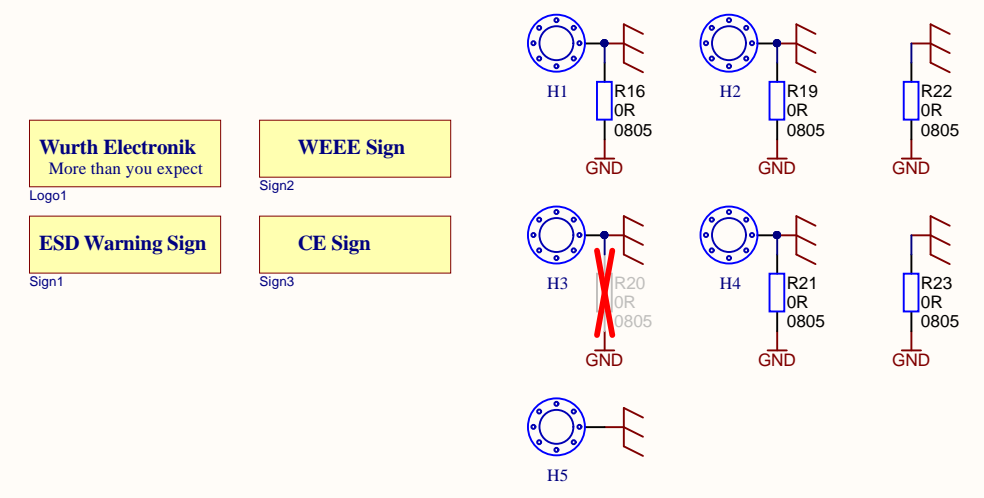
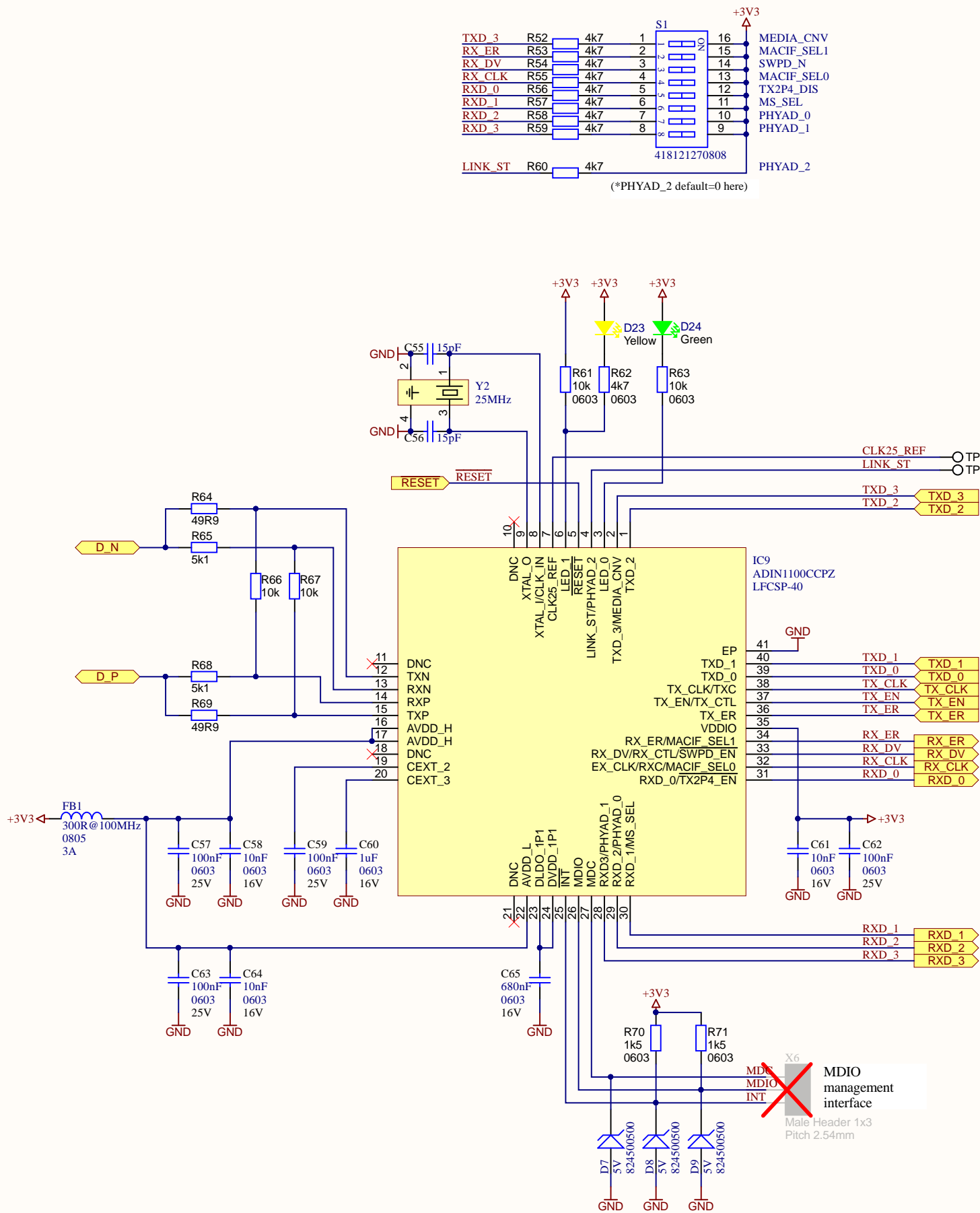


Table 2. LTC9111 Class Configuration

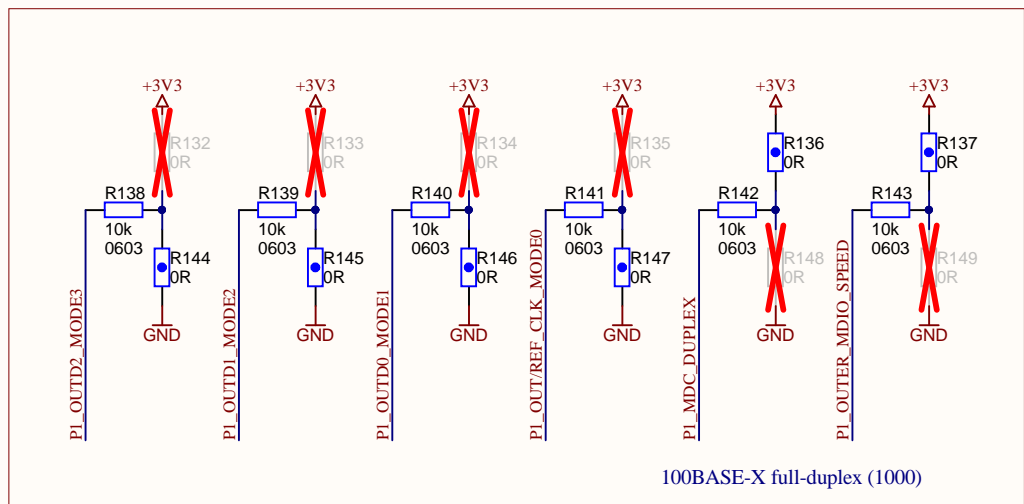
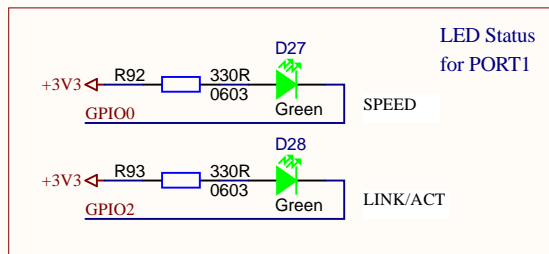
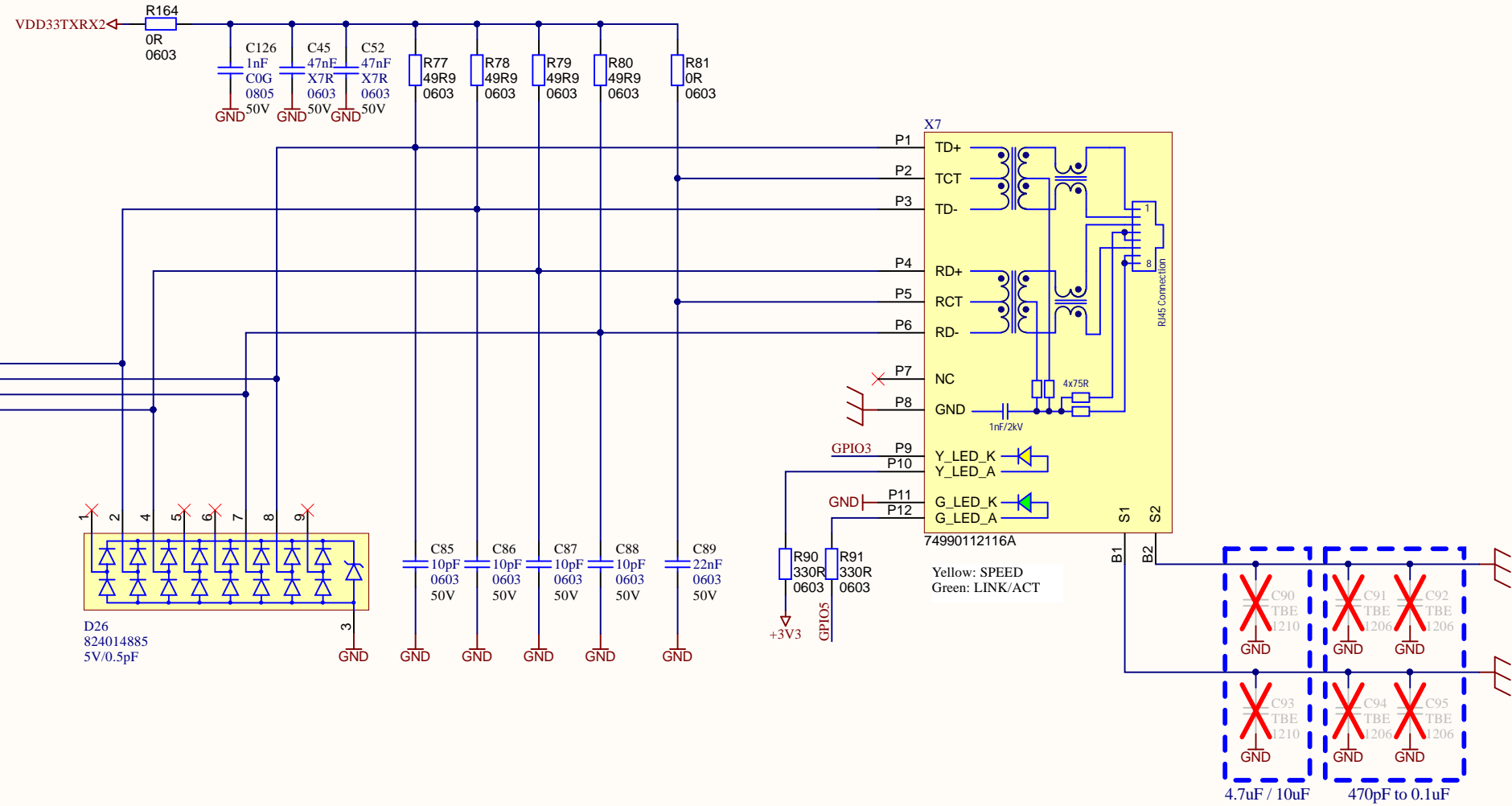
PD CLASS	CLASSV	CLASSC
10	GND	GND
11	GND	FLOAT
12	GND	STBY
13	STBY	GND
14	STBY	FLOAT
15	STBY	STBY



ADIN1100 HARDWARE CONFIGURATION



Rev.	Content	Date	Name	WÜRTH Elektronik eiSos			
1.0	Original Document	01-01-2023	Nattawut	PoDL ADIN1100 10BASE-T1L PHY			
1.1	Change to AD controller	20-04-2023	Nattawut				
1.2	Update Power Coupling	04-11-2023	Nattawut	Customer:			
1.3	Improve for EMC ability	14-05-2024	Nattawut				
1.4	Add D31, Replace FB7 to R164	05-07-2024	Nattawut	Size A3	Document Number 02-10BASE-T1L_PHY.SchDoc	Modified By: Nattawut	Rev 1.5
1.5	Improve for EMC ability	16-09-2024	Nattawut	Print Date : 19/09/2024 Design Date : Mon 1st Aug, 2020 Sheet: 2 of 4			



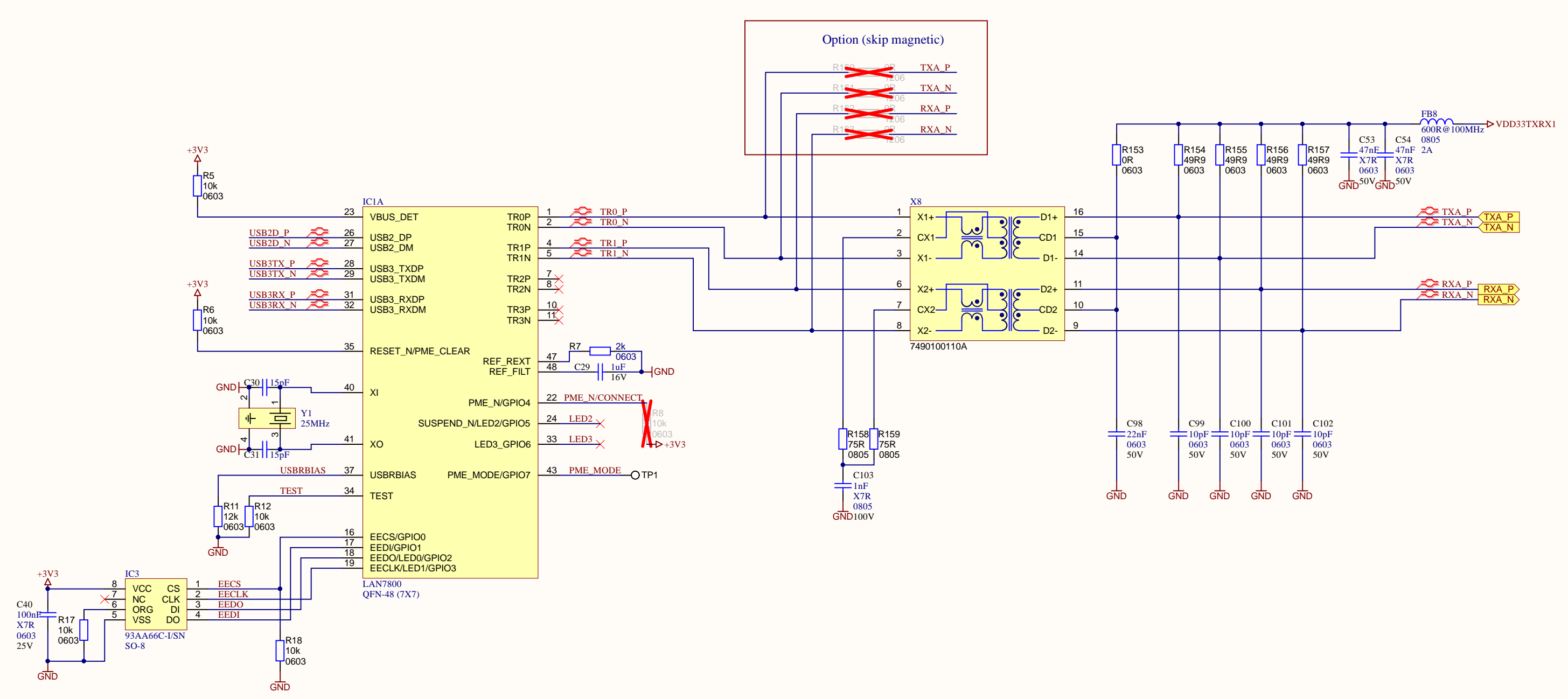
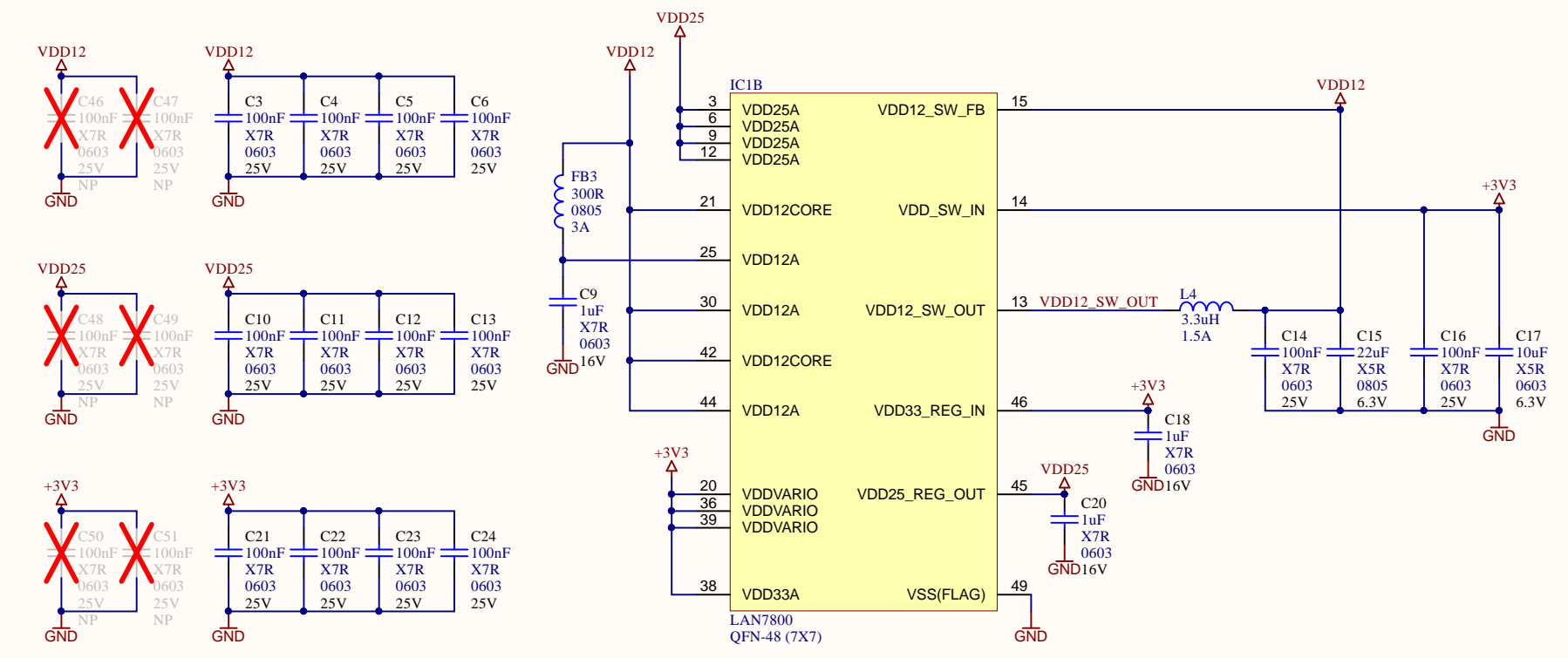
P1_INTPHY : P1_MODE3	P1_MODE2	P1_MODE1	P1_MODE0	Port 1 Mode
00	0	x	x	MII MAC
00	1	0	x	MII PHY
00	1	1	0	Turbo MII PHY 12 ma
00	1	1	1	Turbo MII PHY 16 ma
01	0	0	x	RMII MAC clock in
01	0	1	0	RMII MAC clock out 12ma
01	0	1	1	RMII MAC clock out 16ma
01	1	0	x	RMII PHY clock in
01	1	1	0	RMII PHY clock out 12ma
01	1	1	1	RMII PHY clock out 16ma
1x	x	x	x	Internal PHY


WÜRTH Elektronik eiSos



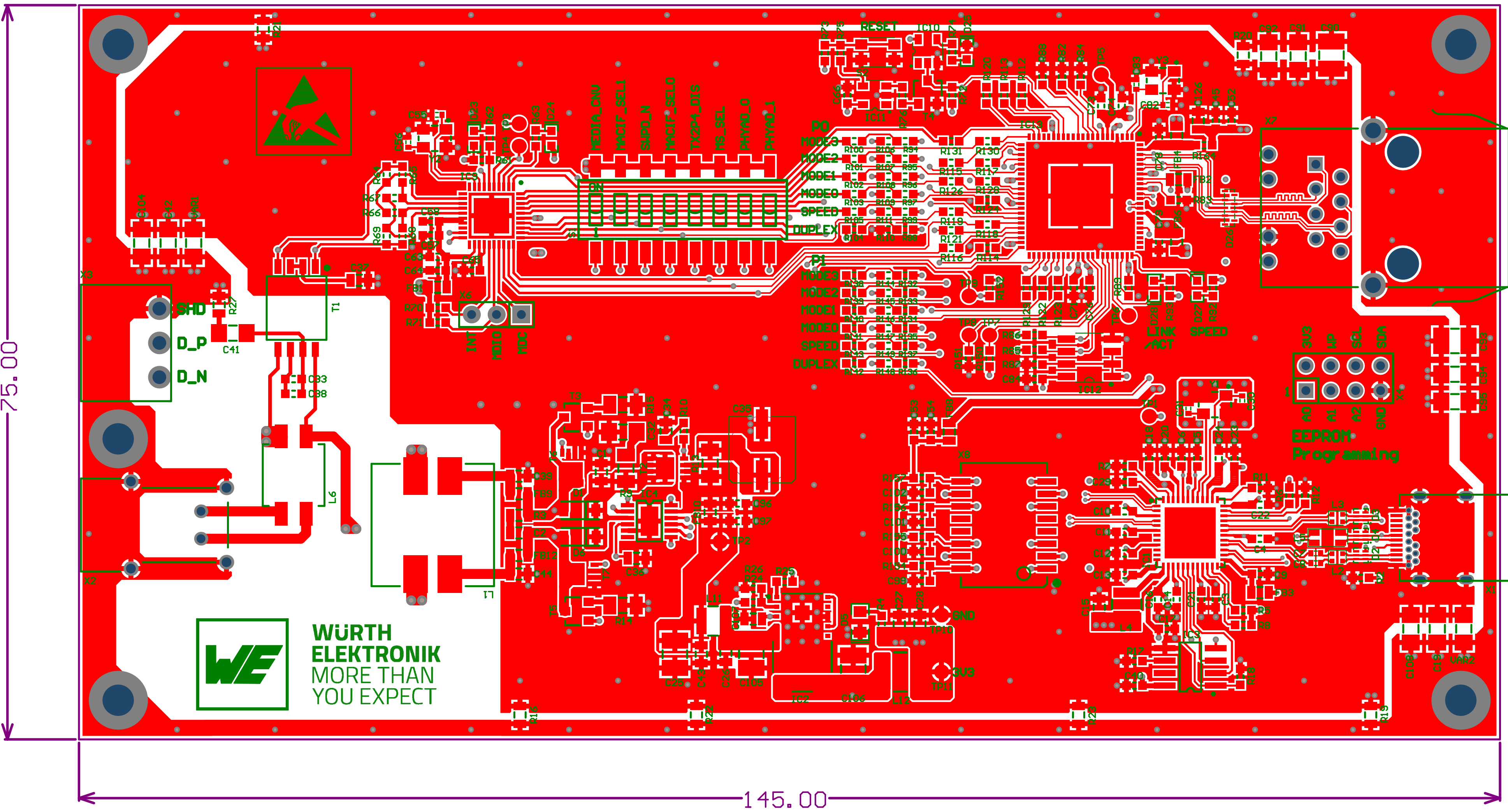
### B TYPE-C Port

The diagram illustrates the internal wiring of a USB-C Receptacle. The receptacle is a yellow component with pins labeled A1 through A12, B1 through B4, and SH1 through SH4. It is connected to a USB-C connector (X1) with pins labeled A4, A9, B4, B9, A2, A3, B11, B10, A10, A11, B3, B2, A6, A7, B7, B6, A5, B5, A8, B8, and D+ through D-. The circuit includes three diode buffers (D2, D3, D4) and two 7442335600 and 744232090 90R @ 100MHz components. It also shows various capacitors (C19, C108, C7, C8) and a resistor (R2).



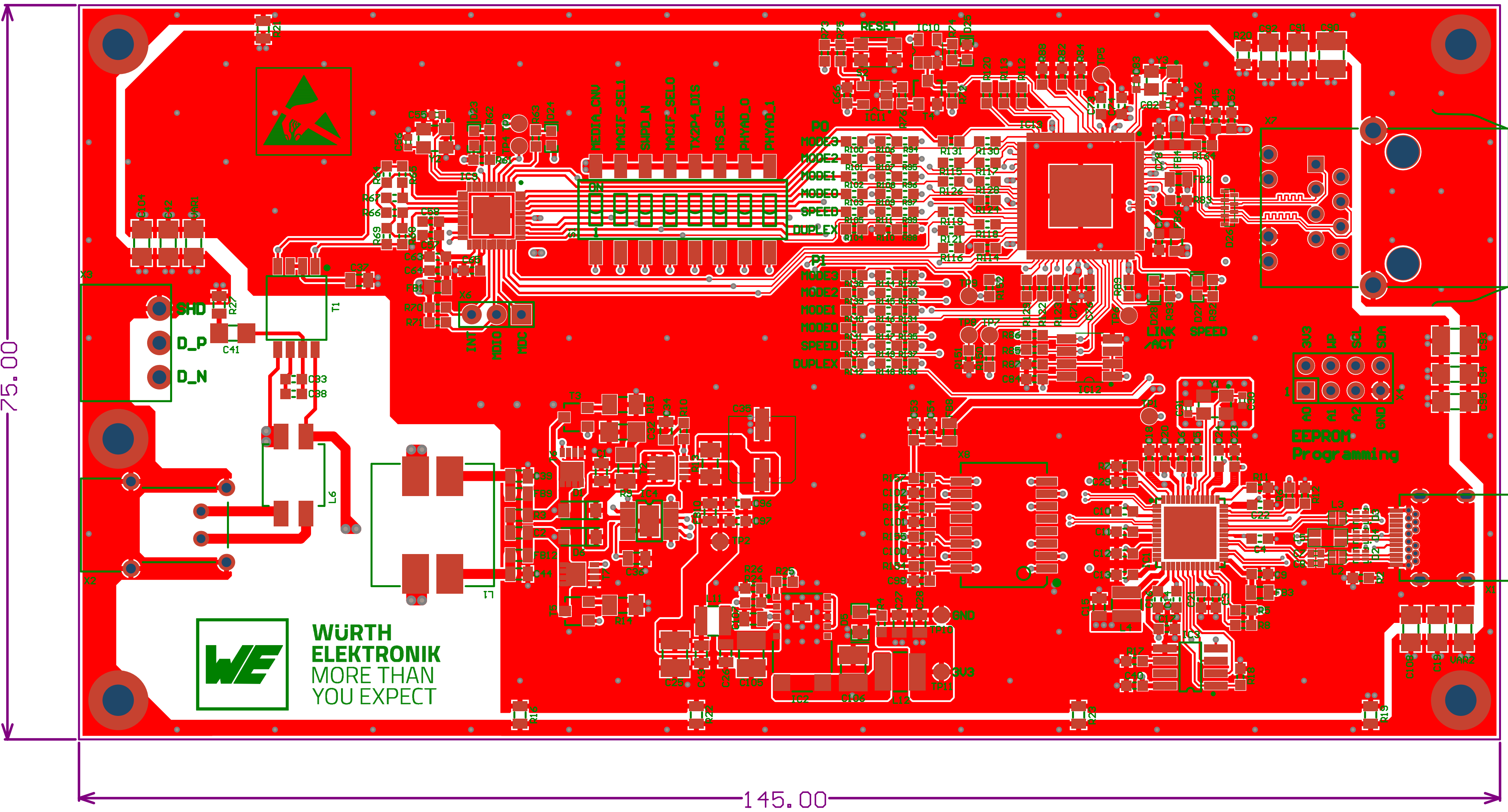
Rev.	Content	Date	Name	<div>  </div>			
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1.4	Add D31, Replace FB7 to R164	05-07-2024	Nattawut				
1.5	Improve for EMC ability	16-09-2024	Nattawut				
				PoDL LAN to USB-C		Customer:	
				Size A3	Document Number 04-LAN-to-USB-C-SchDoc	Modified By: Nattawut	Rev 1.5
				Print Date : 19/09/2024		Design Date : Mon 1st Aug, 2020	
				Sheet: 4 of 4			

Top Layer



Layer	Name	Material	Thickness	Constant	Board Layer Stack
1	Top Overlay				
2	Top Solder	Solder Resist	0.010mm	3.8	
3	Top Layer	Copper	0.035mm		
4	Dielectric 1	7628	0.210mm	4.6	
5	Signal Layer 2	Copper	0.015mm		
6	Dielectric 3	Core-009	1.065mm	4.6	
7	Signal Layer 3	Copper	0.015mm		
8	Dielectric 2	PP-006	0.210mm	4.6	
9	Bottom Layer	Copper	0.035mm		
10	Bottom Solder	Solder Resist	0.010mm	3.8	
11	Bottom Overlay				

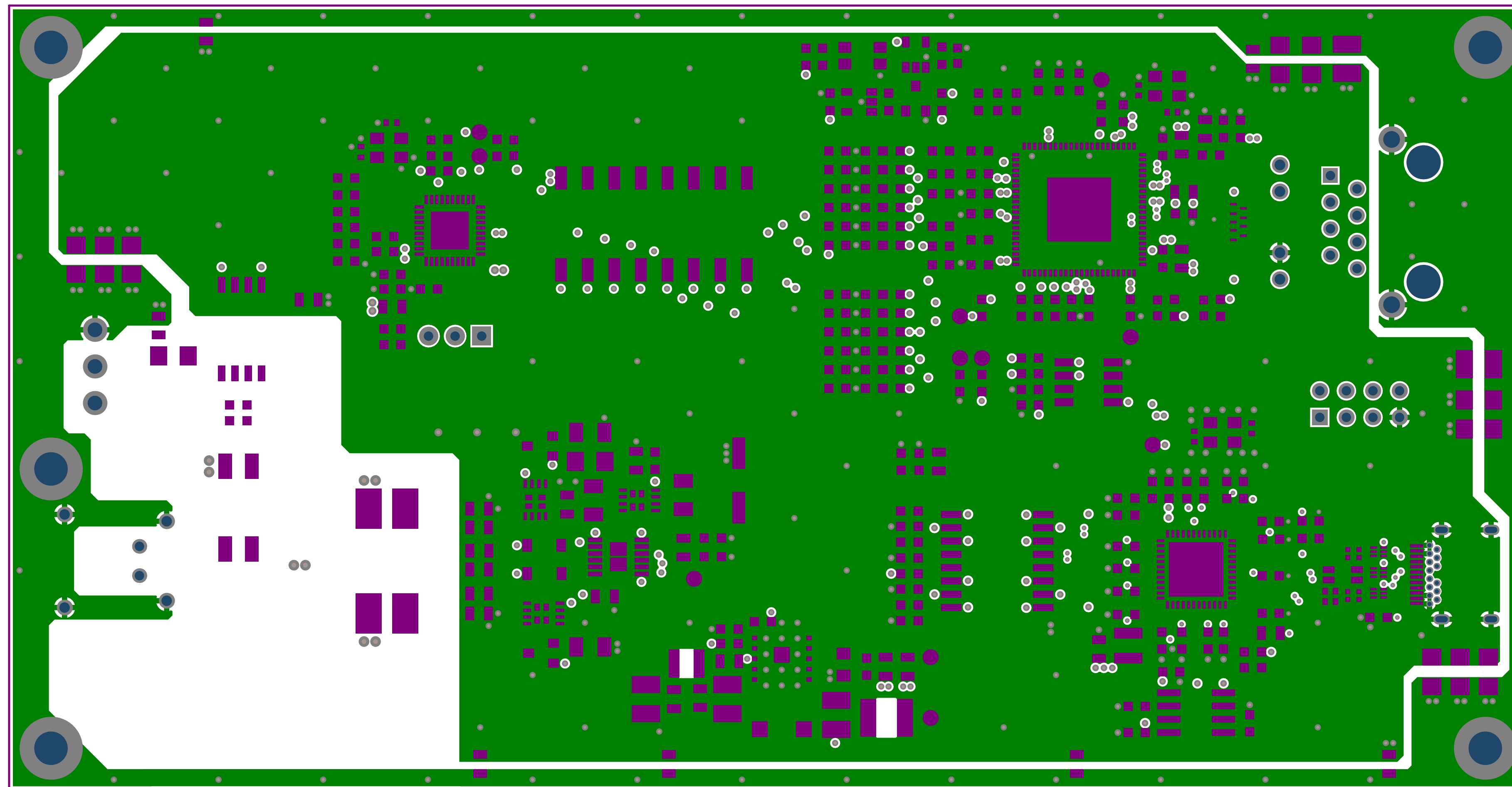
Top Layer



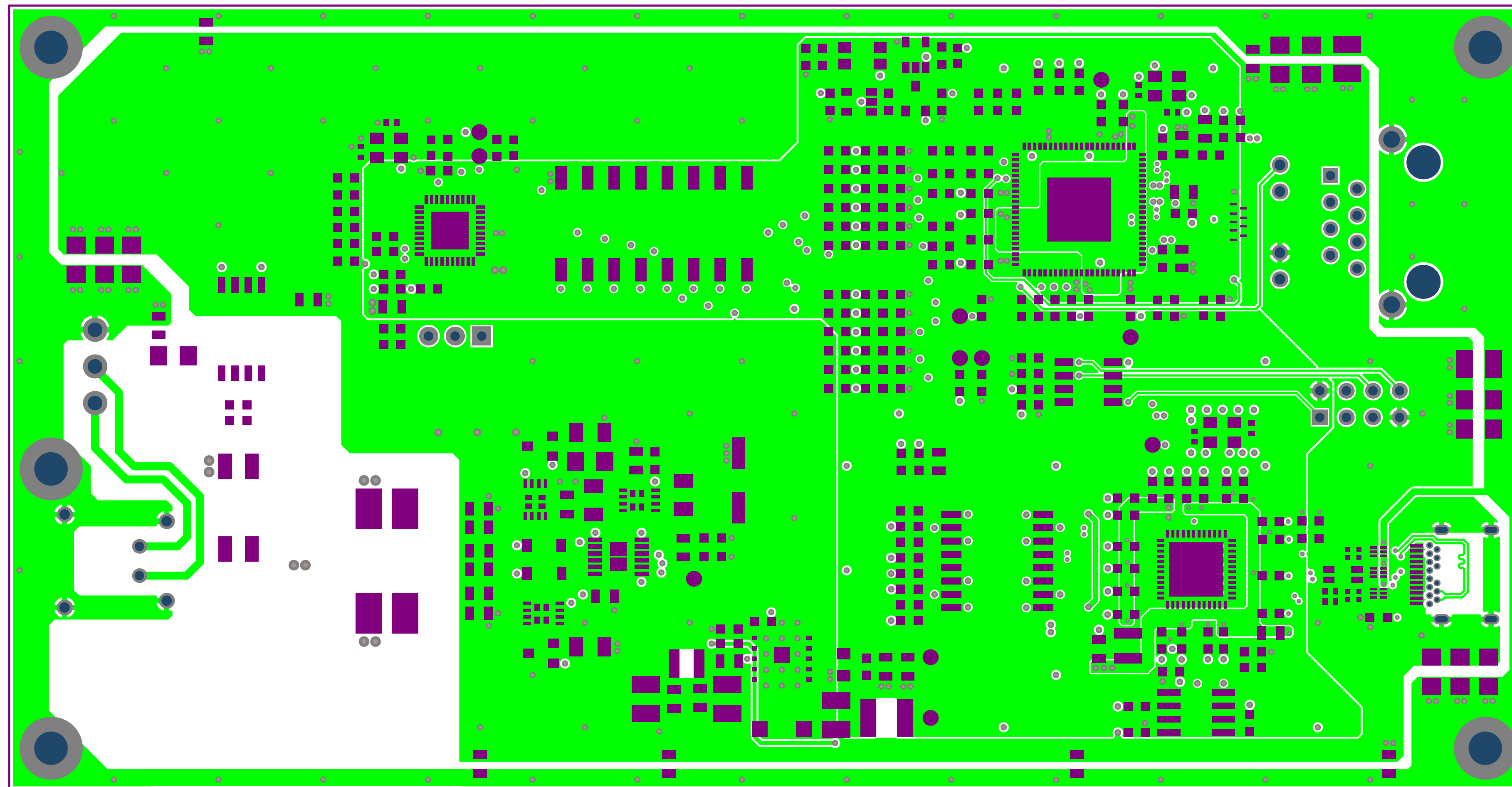
Layer	Name	Material	Thickness	Constant	Board Layer Stack
1	Top Overlay				
2	Top Solder	Solder Resist	0.010mm	3.8	
3	Top Layer	Copper	0.035mm		
4	Dielectric 1	7628	0.210mm	4.6	
5	Signal Layer 2	Copper	0.015mm		
6	Dielectric 3	Core-009	1.065mm	4.6	
7	Signal Layer 3	Copper	0.015mm		
8	Dielectric 2	PP-006	0.210mm	4.6	
9	Bottom Layer	Copper	0.035mm		
10	Bottom Solder	Solder Resist	0.010mm	3.8	
11	Bottom Overlay				



Inner Layer2 (GND Plane)



Inner Layer 3 (Power/GND Plane)







## Bottom Layer

